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EXAMINER	
WONG, XAVIER S	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/627,486	KIM, YOUNG SUCK	
	Examiner	Art Unit	
	Xavier Szewai Wong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24th April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Claims **1**, **2**, **3**, **7**, **10**, **16** – **21**, **25**, **26** and **27** have been amended
- Claims **1** – **31** are pending in the present application with claim **31** being new

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *24th April 2008* has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims **1**, **2**, **3**, **7 – 10**, **14 – 20**, **25**, **26**, **27** and **31** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kantola** et al (**US 5,963,634**) in view of **Aschermann** (**US 2003/0026202 A1**).

2. Claims **1**, **2**, **3**, **10**, **16 – 20**, **25**, **26**, **27** and **31**: **Kantola** et al show in figure *3* a redundant switching system wherein a first unit (WO) is mirrored to a second unit (SP) in real-time (abstract; col. *6* ln. *60-67*, col. *7* ln. *1-2*), wherein the first unit (WO) comprises a switching unit for transferring the routing information from the first unit to the second unit (SP) (col. *7* ln. *2-8*), eliminating a delay associated with the use of a PCI-to-PCI board (i. *real-time* switching ii. no where in the reference mentions PCI), wherein the mirrored routing information is transferred along one path from a first switching unit of the first unit (WO) directly to a second switching unit (SP) (fig. *3*, $W_{wo} \rightarrow W_{sp}$ is a direct link). Further, **Kantola** et al disclose that the σ^{wo} of the first unit and the σ^{sp} in the second unit comprise memories (queues) that store routing information to be transferred to and received by the first and second units respectively (col. *9* ln. *40-49*, col. *11* ln. *48-51*); enabling copying of routing information (files) from an active (WO) unit to a spare (SP) unit and may continue updating data while copying is going on a real-time switching (col. *5* ln. *18-39*, col. *6* ln. *18-21*), such functionality reads on as simultaneously transferring information between the two units. However, **Kantola** et al may not have specifically mentioned the first and second switching units comprises at least one *PLD* for controlling the at least one switching unit. Aschermann teaches in figure *2B* a redundancy peripheral units system wherein peripherals 100_A and 100_B each comprising a redundancy/radio link controller (102_A & 102_B) wherein the controllers are ASICs (e.g. PLDs, [0040, 0046]). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to modify or implement the ASIC (PLD) controllers of **Aschermann** to the W_{wo} and W_{sp} portions of **Kantola** et al for convenient reprogramming of the controllers to accommodate different traffic between the units.

Claims **7** and **14**, applied to claims **1** and **10**: **Kantola** et al teach two switching units but may not have very specifically mentioned that the switching units being programmable. **Aschermann** teaches redundant peripherals employ programmable logic circuits ([0046]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify or implement the switching units of Kantola et al to become programmable as taught by **Aschermann** for convenient reconfiguring the switching units to accommodate different traffic between the units.

Claims **8** and **15**, applied to claims **7** and **10**: **Kantola** et al and **Aschermann** show first and second units are structural equivalents (**Kantola** fig. *3* & **Aschermann** figs. *2B* or *7*).

Claim **9**, applied to claim **7**: **Aschermann** further teaches that the first and second units are functional equivalents since it is a redundant system ([0010]).

Claims **22**, **23**, **24**, **29** and **30** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kantola** et al (**US 5,963,634**) in view of **Aschermann** (**US 2003/0026202 A1**), as applied to claims **21**, **22**, **25** and **29**, and in further view of **Saine** et al (**US 6,014,504**).

Claims **22**, **23**, **24**, **29** and **30**, applied to claims **21**, **22**, **25** and **29**: **Kantola** et al, as modified by **Aschermann**, disclose the claimed invention but not the structure of the switching unit comprising a 2:1 MUX wherein when a select signal of the MUX is in a first state, the MUX outputs a first signal, and when the select signal is in a second state, the MUX outputs a second signal; and, a tristate output buffer is connected to the output terminal of the MUX and wherein the select signal is equal to a first value, the tristate output buffer is in an output-enable state and when the select signal is equal to a second value, the tristate output buffer is in an output-disable state. **Saine** et al show in figure *4* items *37*, a 2:1 MUX (2 inputs, 1 output, 1 control terminal responsive to a select signal), connected to item *38a*, a tristate output buffer; wherein the select signal selects between normal (first state → first signal) or desired fault data (second state → second signal) (col. *4* ln. *61-65*); wherein the tristate output buffer is controlled by a WRITE signal which tells the tristate output buffer whether to write data (first value – output enable) to data lines or not to write (second signal – output disable) to the data lines (col. *5* ln. *1-4*). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the MUX and tristate output buffer of **Saine** et al to the switching units of **Kantola** et al, as modified by **Aschermann**, to control traffic flow.

Claims **21** – **24**, **28** and **30** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kantola** et al (**US 5,963,634**) in view of **Aschermann** (**US 2003/0026202 A1**), as applied to claims **16**, **21**, **25** and **29**, and in further view of **Asfour** (**US 5,182,801**).

Claims **21** and **28**, and as applied to claims **16** and **25**: **Kantola** et al, as modified by **Aschermann**, disclose the claimed invention. However, there are no mentioning of *a tri-state buffer in communication with a multiplexer*; wherein the first switching unit is configured to *connect a plurality of external devices to route signal inputted from a first device to a second device according to control information*. **Asfour** illustrates in fig. *4* that a (first) switch *40* with a multiplexer (MUX *81* or *82*) in communication with a tri-state buffer (*86a* or *86b*); and in fig. *1* the switch unit *40* is coupled to external devices *10* & *11,* which are connected to each other; wherein (first) device *10* may send a request to (second) device *11* and a control logic *50* as the control arbitrates a decision (col. *4* ln. *4-10*; col. *8* ln. *4-19*). It would have been obvious to one of ordinary skill in the art to incorporate the structure of **Asfour**, in the system and method of **Kantola** et al as modified by **Aschermann**, for data transfers between devices.

Claims **23**, **24** and **30**, applied to claims **22** and **29**: **Kantola** et al as modified by **Aschermann**, disclose the claimed invention except explicitly mentioning a multiplexer outputting a first signal when a select signal is in a first state; and outputting a second signal when the select signal is in a second state; wherein when the select signal is a first value, the tri-state buffer is in output-enable state, and when select signal is a second value, the tri-state buffer is in output-disable state. **Asfour** discloses control signals (through decode logic *49* → select signal; line *85a* in fig. *4*) are applied to the multiplexer *82* and tri-state output buffer *87a* to route connection to <u>any</u> (therefore; may be in 1. <u>connected state</u>; or 2. <u>not-connected state</u>) memory ports (col. *6* ln. *41-46*). Therefore, when a (first) signal is output from the multiplexer, the tri-state buffer can

accordingly be in a first (output-enable/connected or output-disable/not-connected) state; when a (second) signal is output from the multiplexer, the tri-state buffer can accordingly be in a second (output-disable/not-connected or output-enable/connected) state. It would have been obvious to one of ordinary skill in the art to incorporate the structure **Asfour**, in the system and method of **Kantola** et al as modified by **Aschermann**, for memory management purposes.

5. Claims **4**, **5**, **11** and **12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kantola** et al (**US 5,963,634**) in view of **Aschermann** (**US 2003/0026202 A1**), applied to claims **3**, **2** and **10** respectively, and in further view of **Tada** (**US 6,487,169 B1**).

Claims **4**, **5**, **11** and **12**, applied to claims **2** and **3**: **Kantola** et al, as modified by **Aschermann**, disclose the claimed invention except routing information being stored in a second memory the second switching unit prevents signal transmission to the second memory; and, when the first memory is loaded, the first switching unit prevents signal transmission to the second unit. **Tada** further discloses that every active (first) or standby (second) switch operation is performed synchronously (col. *3* ln. *21-23*); therefore, no interruption during transmission translates to no signal is transmitted from either first or second switches. Furthermore, **Tada** mentions as the active (first) switch reads out/transmits all its cells to the standby (second) switch (from a full load) after a time tip and cells are written into a buffer in the standby switch (col. *4* ln. *18-49*); therefore, no signal interrupts the buffer memory while transmission is in progress. It would have

been obvious to one of ordinary skill in the art to program the switching units to prevent (e.g. read, write) interruptions taught by **Tada**, in the switching units of **Kantola** et al, as modified by **Aschermann**, in order to prevent read and write conflict.

7. Claims **6** and **13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kantola** et al (**US 5,963,634**) in view of **Aschermann** (**US 2003/0026202 A1**) and **Tada** (**US 6,487,169 B1**), as applied to claims **5** and **12**, and in further view of **Schultz** (**US 6,012,109 B1**).

Claims **6** and **13**, applied to claims **5** and **12**: **Kantola** et al as modified by **Aschermann** and **Tada**, disclose the claimed invention except the second switching unit prevents data from being loaded from the second memory. **Schultz** discloses a concept of preventing write access (read as prevent data from being loaded) from a memory unit by a DMA controller while the memory unit is being read (col. *11* ln. *10-34*). It would have been obvious to one of ordinary skill in the art to apply the concept of not loading memory while memory is being read as taught by **Schultz** to reprogram the switching unit of **Kantola** et al, as modified by **Aschermann** and **Tada**, to prevent data from being loaded from the (second) memory and data collision and read-write inconsistency.

Response to Arguments

13. Applicant's arguments with respect to claims **1**, **16** and **25** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

Eltschka et al (**US 6,883,039 B1**) teach 1:1 redundant unduplicated peripheral devices simultaneously updating the switching data memories and states of virtual peripheral devices of the redundant unit per logic updating channel or updating channel physically present in the peripheral devices

Gao (**US 2005/0002405 A1**) teaches a switching core broadcasts packets by directing the packets and duplicates of the packet to slave user switches that are directly connected to a master user switch

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is 571-270-1780. The examiner can normally be reached on Monday through Friday 8:30 am - 6:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Seema S. Rao/
Supervisory Patent Examiner, Art Unit 2616

Xavier Szewai Wong
X.S.W / x.s.w
23rd May 2008